OFF-state TDDB in High-Voltage GaN MIS-HEMTs

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Purpose

- Further understanding of time-dependent dielectric breakdown (TDDB) in GaN MIS-HEMTs
- Explore TDDB under high-voltage OFF-state conditions: most common state in the operation of a power switching transistor

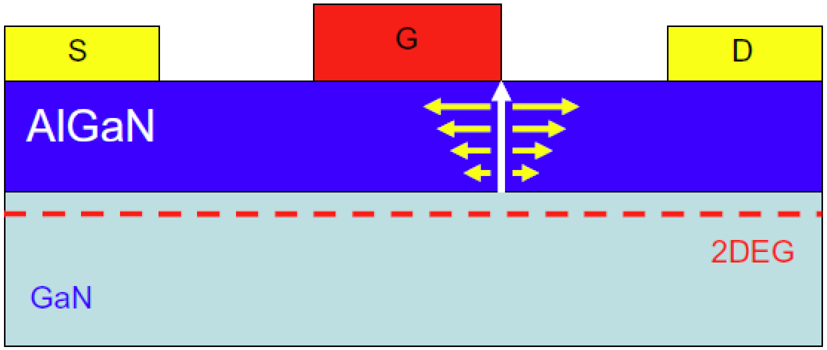
Outline

- Motivation & Challenges
- Initial Results & Breakdown Statistics
- Ultraviolet Light During Recovery & Stress
- Conclusions

Motivation

GaN Field-Effect Transistors (FETs) promising for high-voltage power applications → more efficient & smaller footprint

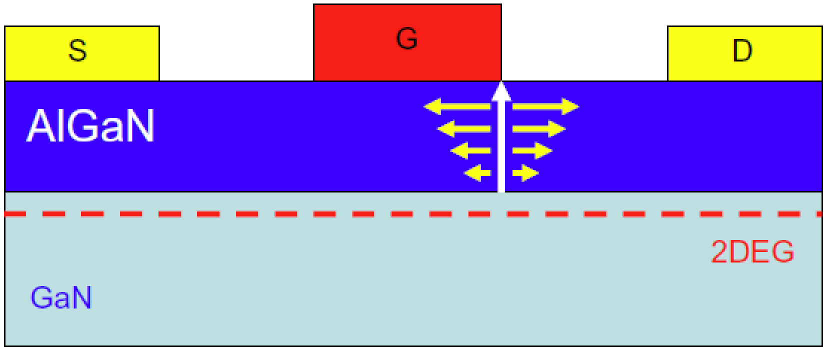
GaN Reliability Challenges



Inverse piezoelectric effect

J. A. del Alamo, MR 2009

GaN Reliability Challenges



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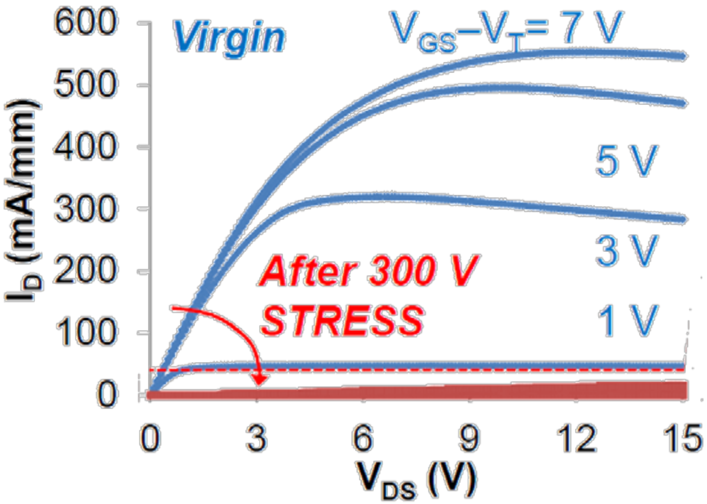
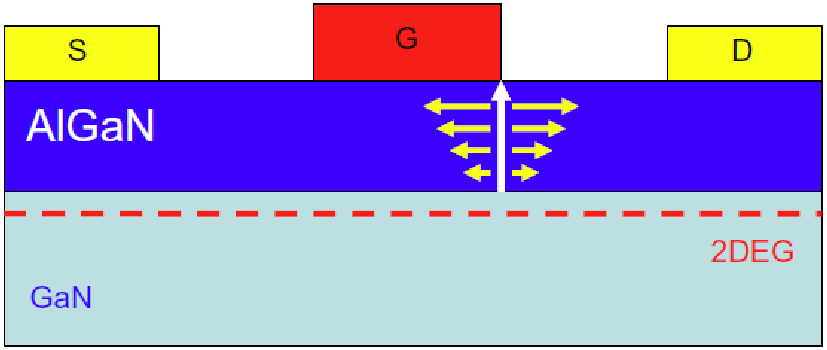


Current collapse

D. Jin, IEDM 2013

GaN Reliability Challenges



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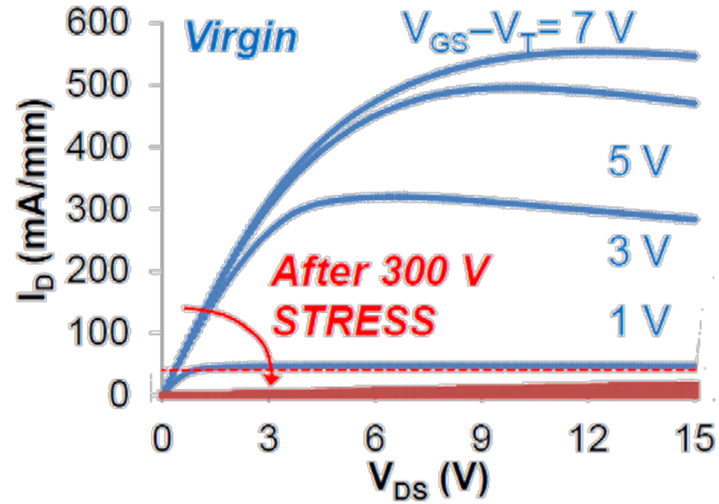
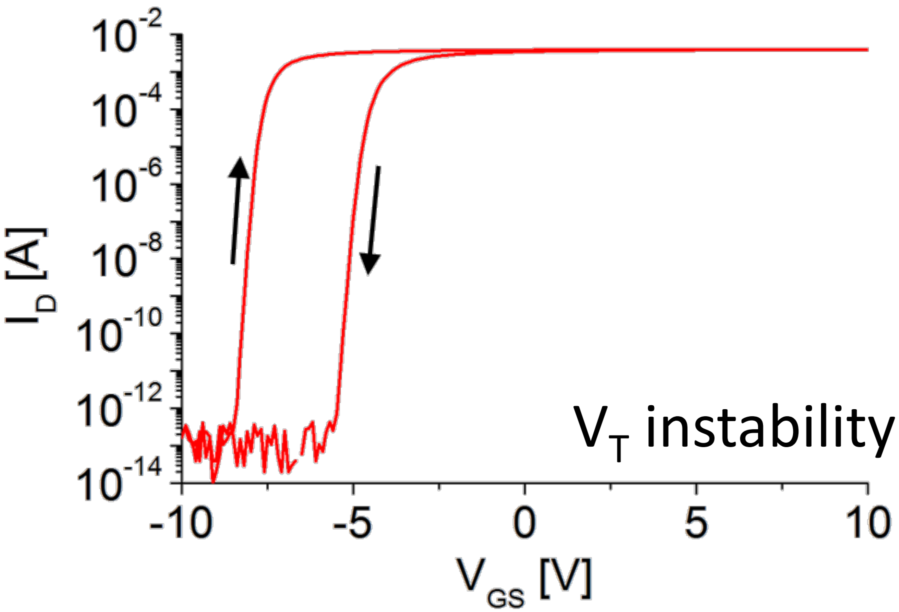


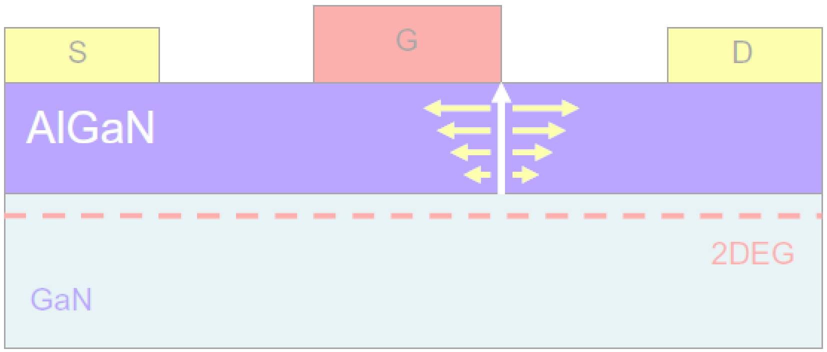
Current collapse

D. Jin, IEDM 2013



V_T instability

GaN Reliability Challenges



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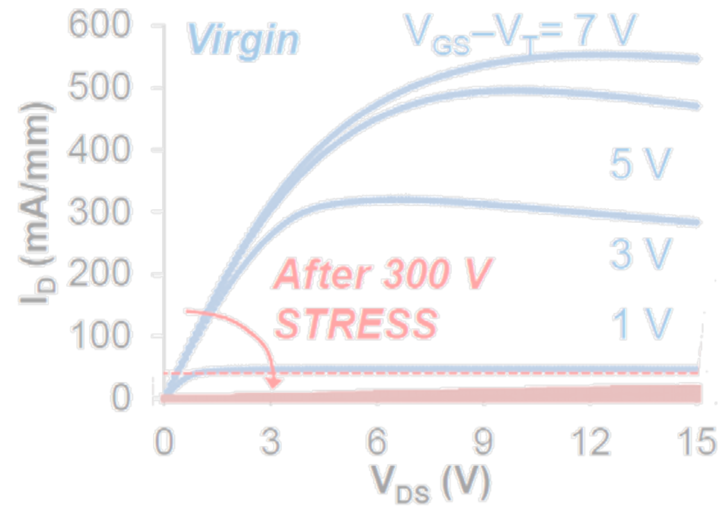
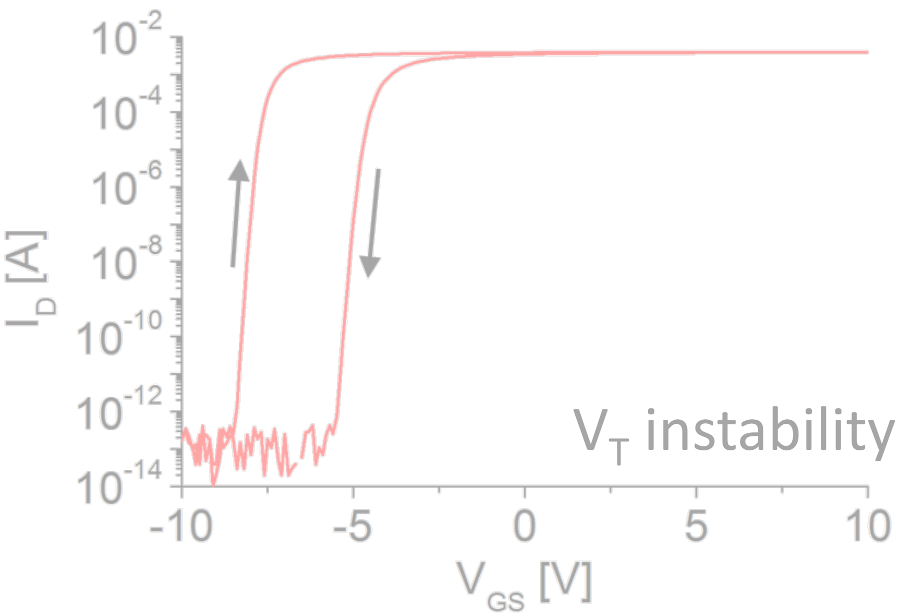


Current collapse

D. Jin, IEDM 2013

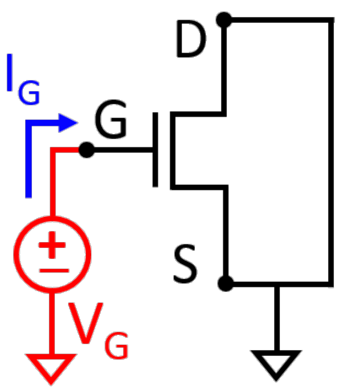


V_T instability

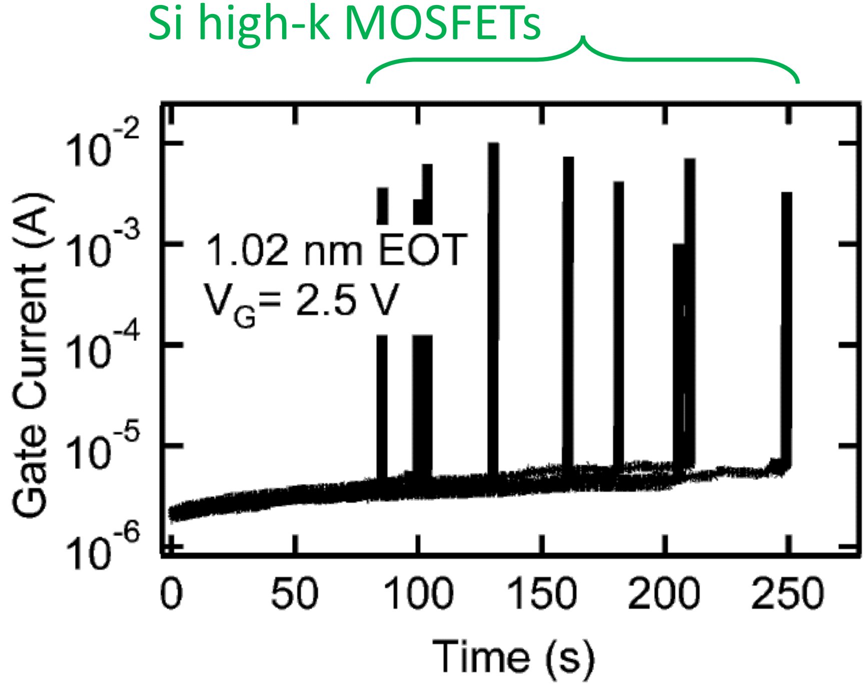
Gate dielectric reliability

Time-Dependent Dielectric Breakdown

- High gate bias → defect generation → catastrophic oxide breakdown
- Often dictates lifetime of chip

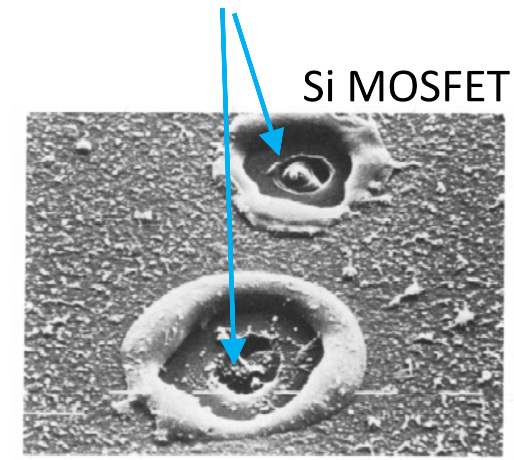


Typical TDDB experiments:
Si high-k MOSFETs



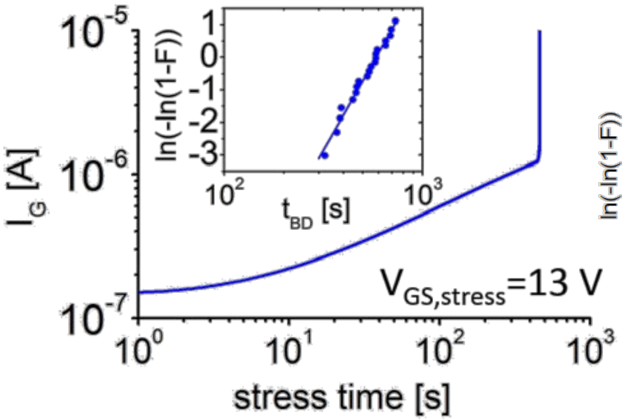
T. Kauerauf, EDL 2005

Gate material melted after breakdown

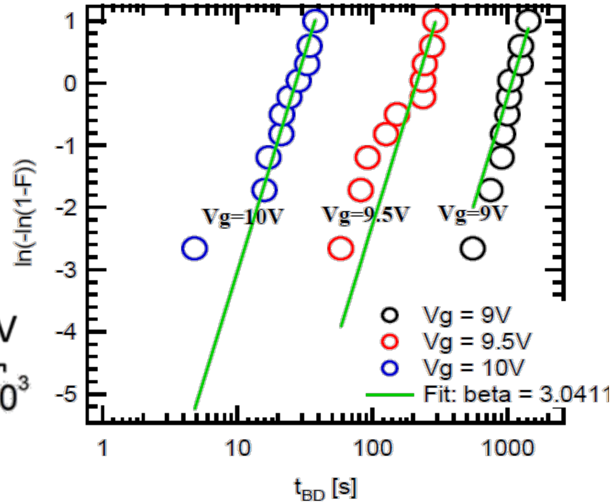


D. R. Wolters, Philips J. Res. 1985

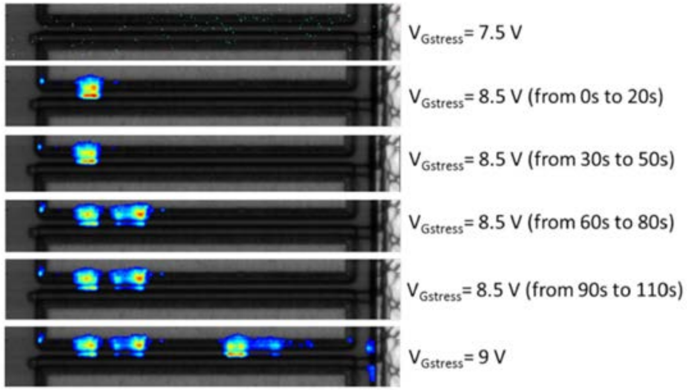
TDDB in GaN MIS-HEMTs



S. Warnock, CS MANTECH 2015



T.-L. Wu, IRPS 2013



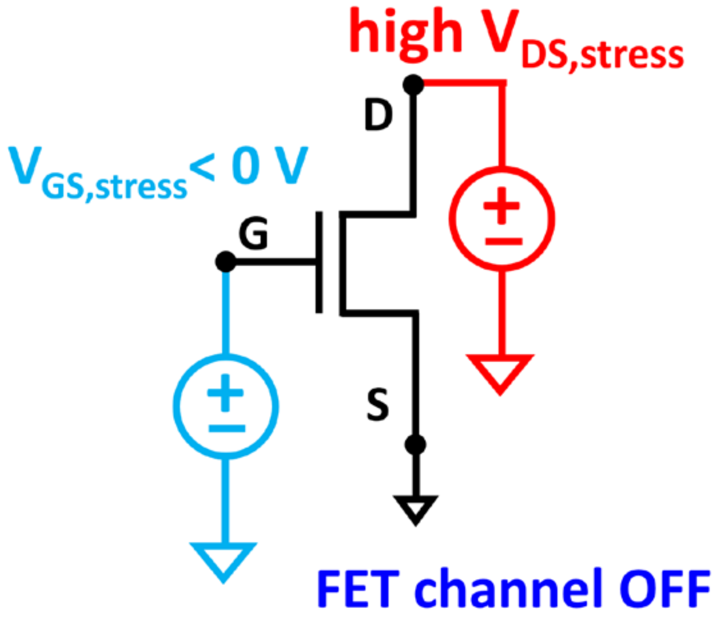
G. Meneghesso, SST 2016

- Classic TDDB observed
- But: studies to date all on positive gate stress TDDB

→ More relevant for D-mode devices: TDDB under OFF-state

OFF-state Stress

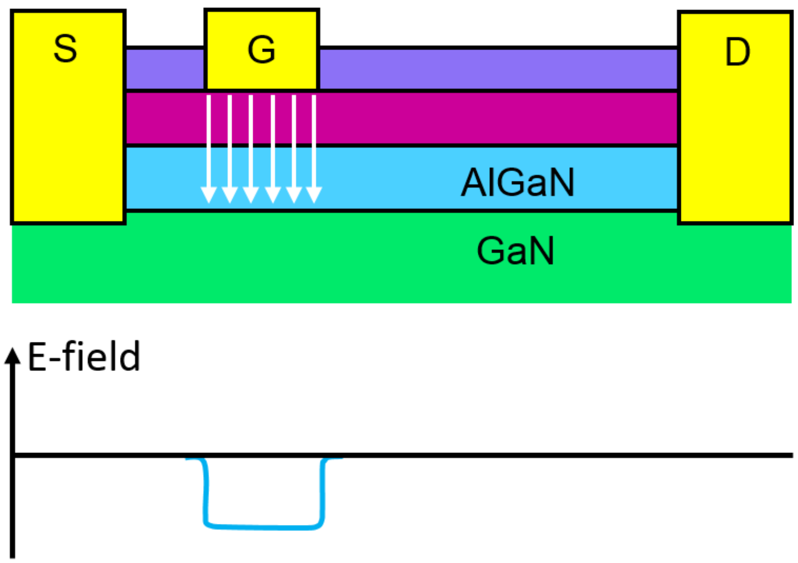
- Negative gate bias turns FET off; high bias on drain
- Relevant operational condition for GaN power circuits



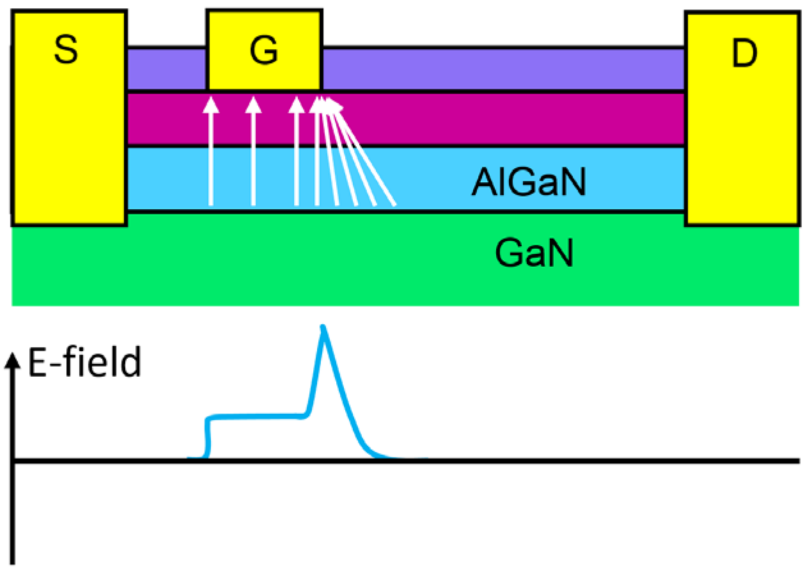
OFF-state Stress

- Negative gate bias turns FET off; high bias on drain
- Relevant operational condition for GaN power circuits
- Electrostatics more complicated than under positive gate stress

Positive gate stress



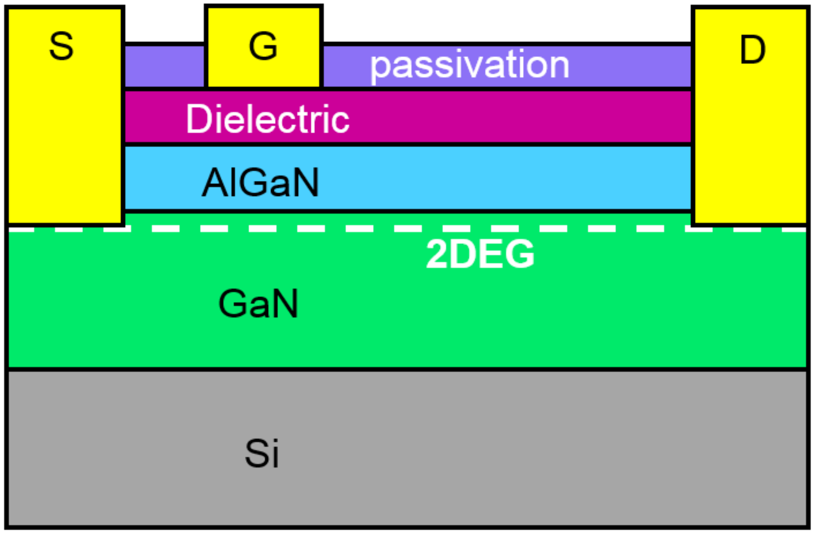
OFF-state stress



- TDDB failure can result from peak in electric field during OFF-state
- Study devices with no field plates for simplicity

Dielectric Reliability in GaN FETs

AlGaN/GaN metal-insulator-semiconductor
high electron mobility transistors (MIS-HEMTs)



Goals of this work:

- What does TDDB look like in the OFF-state stress condition?
- How do transient instabilities (current collapse, V_T shift) affect our ability to observe TDDB?

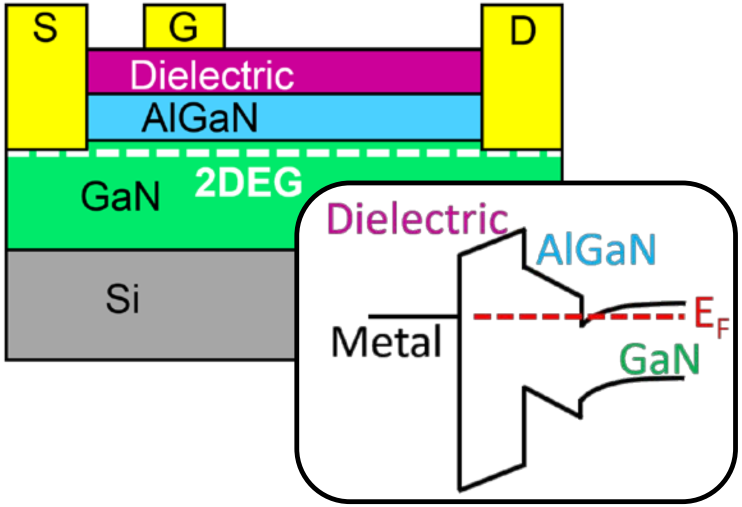
Initial Results & Breakdown Statistics

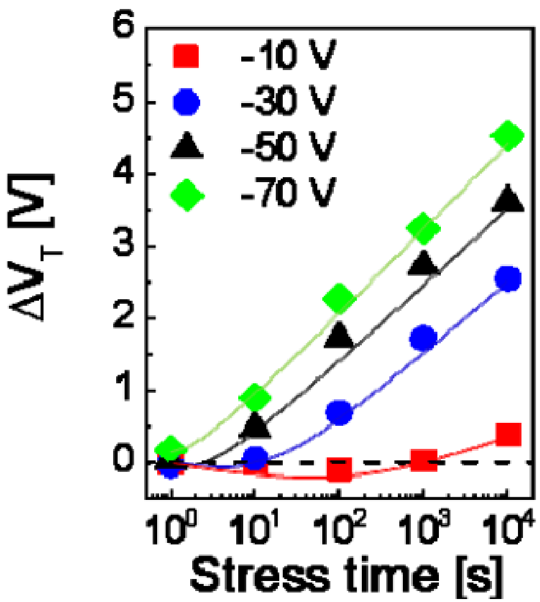
GaN MIS-HEMTs for TDDB Study

- GaN MIS-HEMTs from industry collaboration: depletion-mode

- Gate stack has multiple layers & interfaces
  - → Uncertain electric field distribution
  - → Many trapping sites

- Complex dynamics involved
  - → Unstable and fast changing V_T
  - → Current collapse



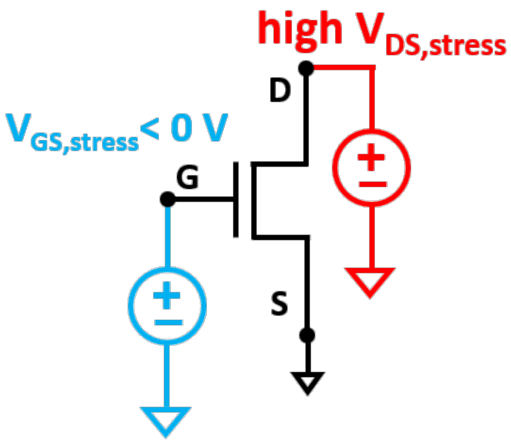


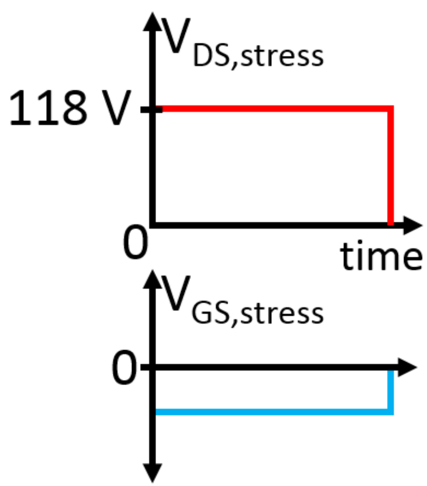
GaN MOSFET

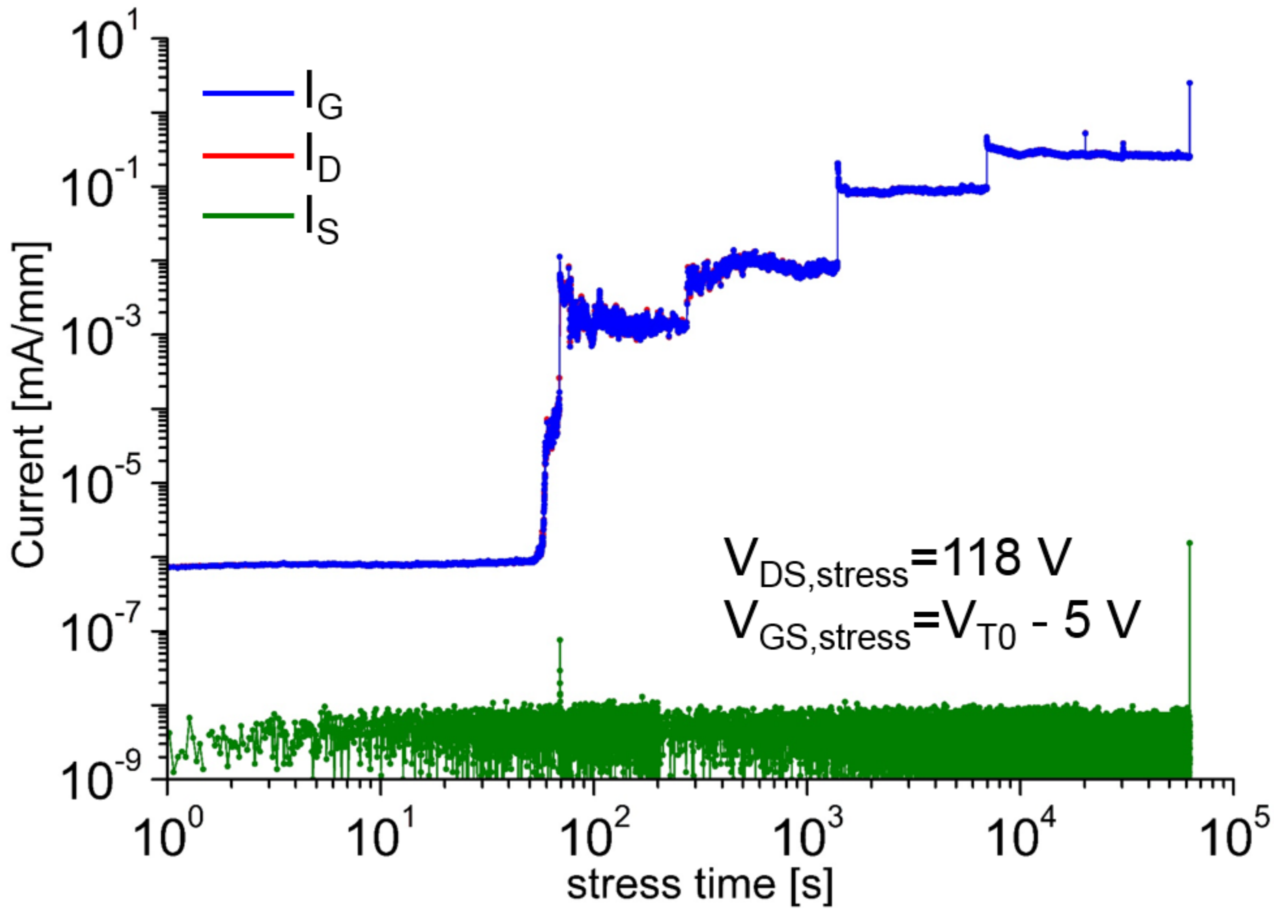
A. Guo, IRPS 2016

Constant-Voltage OFF-state Stress

$V_{GS,stress} < 0$ V, high $V_{DS,stress}$







$I_G = I_D$ → damage at drain-side edge of gate

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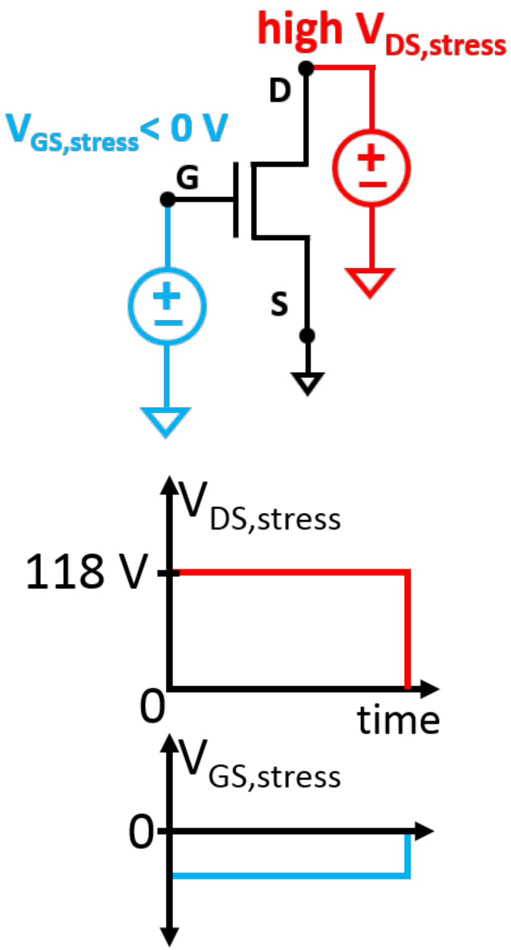

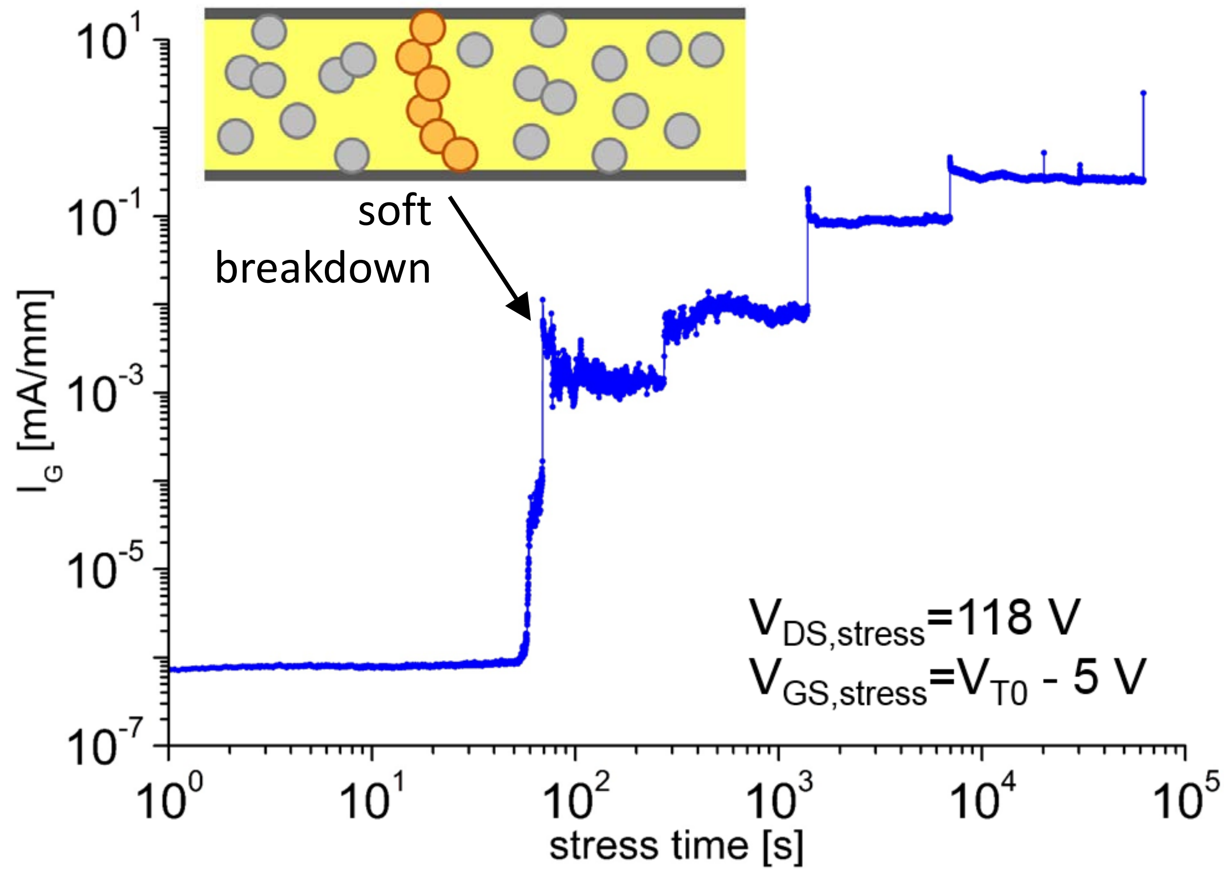

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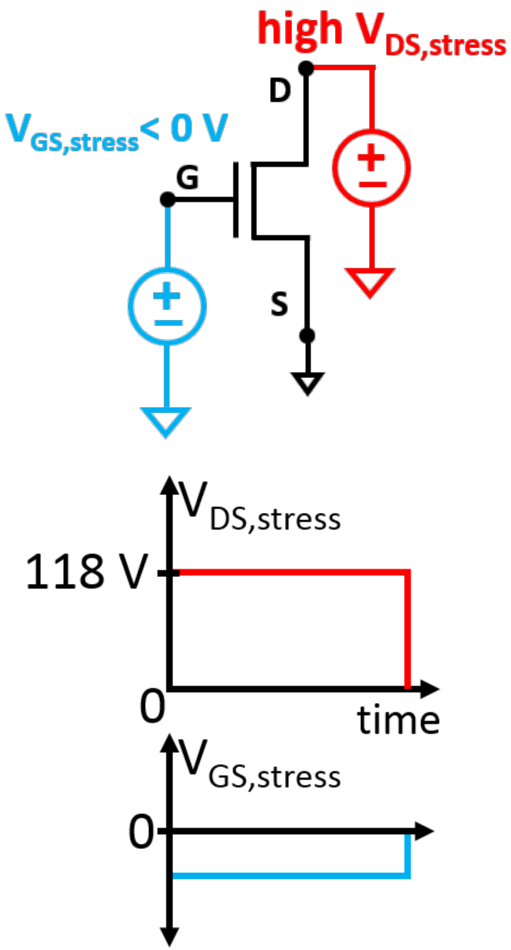
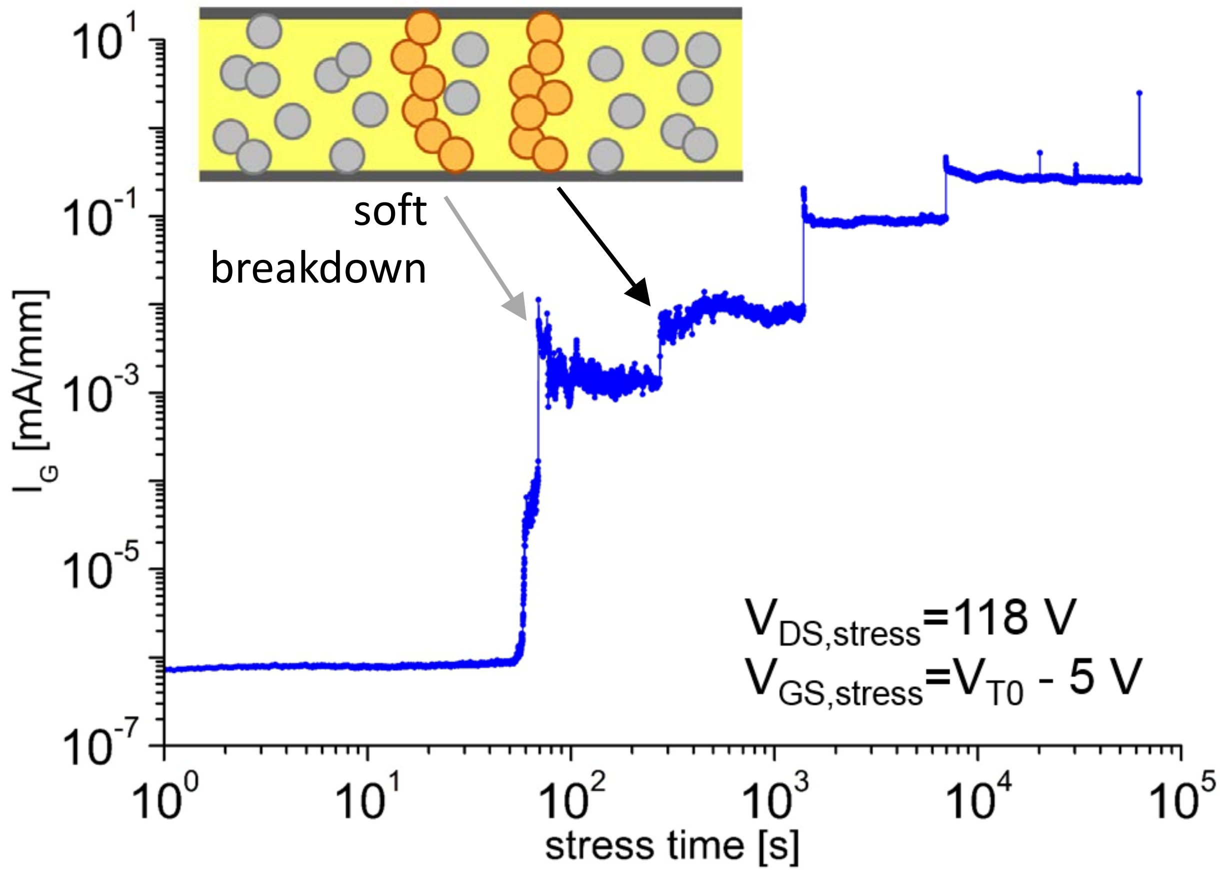
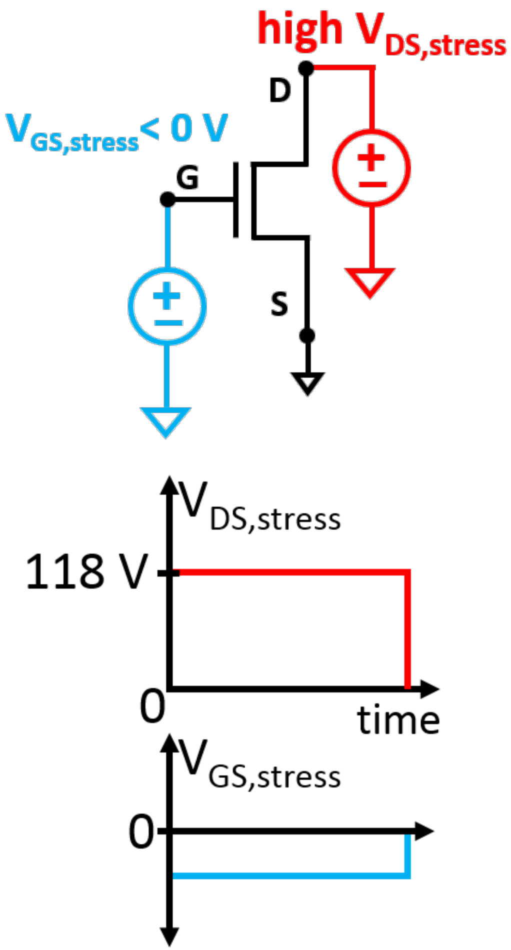


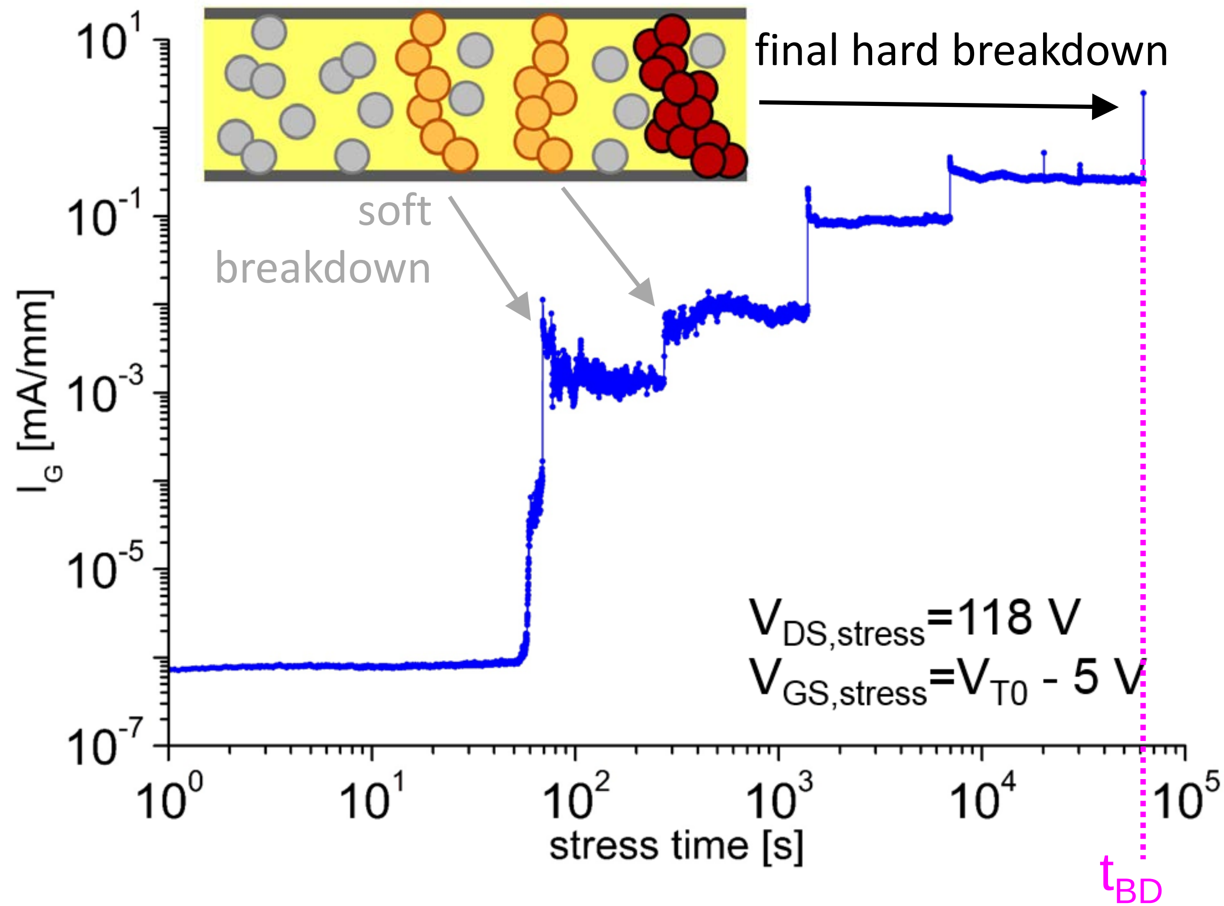


$I_G = I_D \rightarrow$ damage at drain-side edge of gate

Constant-Voltage OFF-state Stress

$V_{GS,stress} < 0$ V, high $V_{DS,stress}$

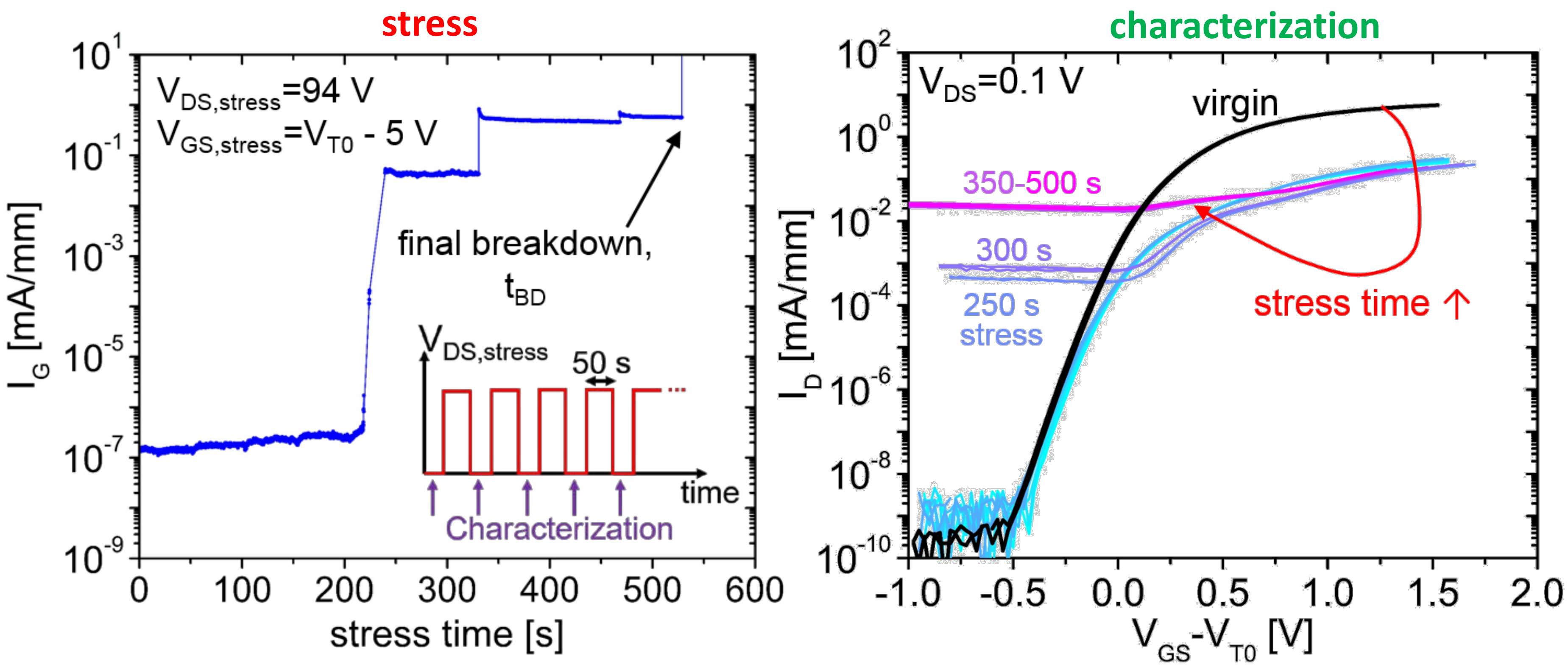




$I_G = I_D$ → damage at drain-side edge of gate

Constant-Voltage OFF-state Stress

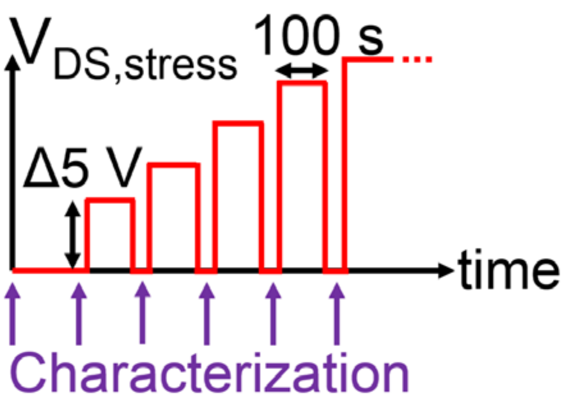
Pause stress every 50 s and characterize device

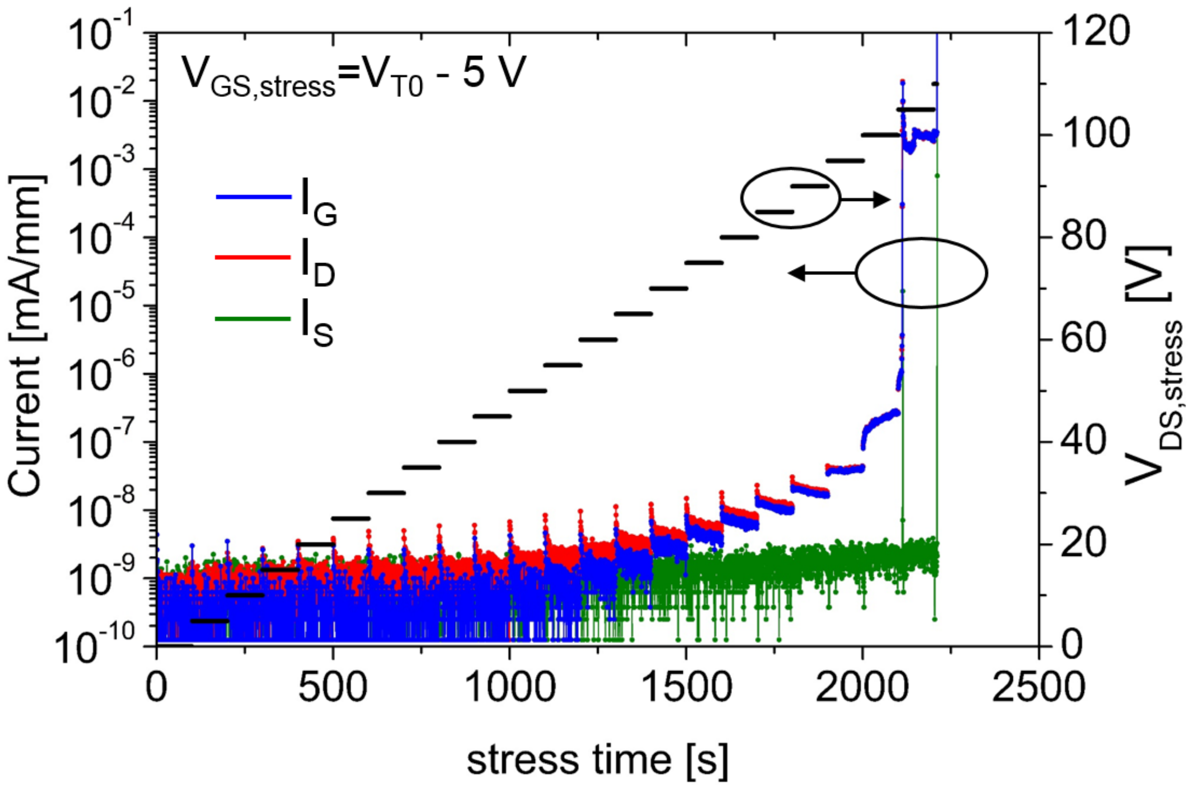


- Multiple jumps in stress I_G before final breakdown
  - Corresponds to increase in I-V OFF-state leakage
- Significant current collapse

OFF-state Step-Stress

Step $V_{DS,stress}$: $\Delta V_{DS,stress}$=5 V, each 100 s/step

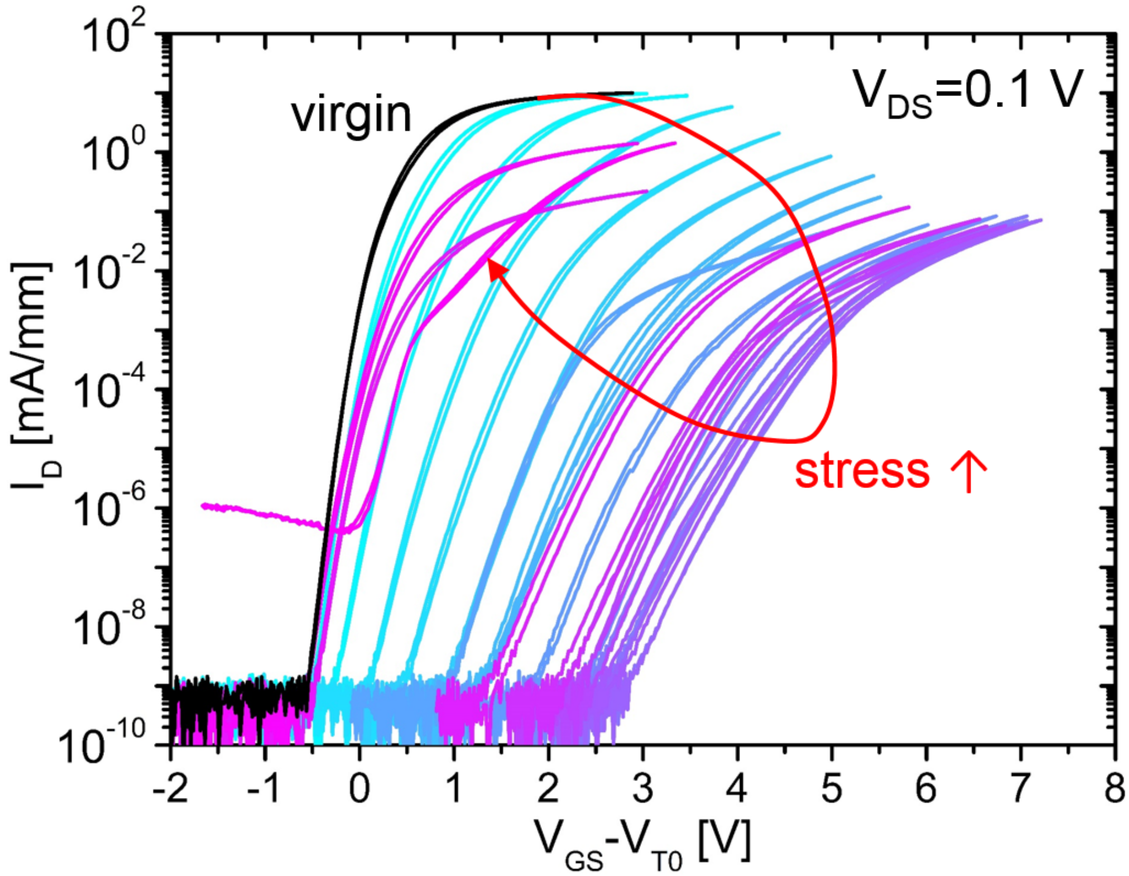




- Moderate stress: I_G=I_D decreases during stress step → trapping
- High stress: I_G increases → stress-induced leakage current (SILC)

OFF-state Step-Stress

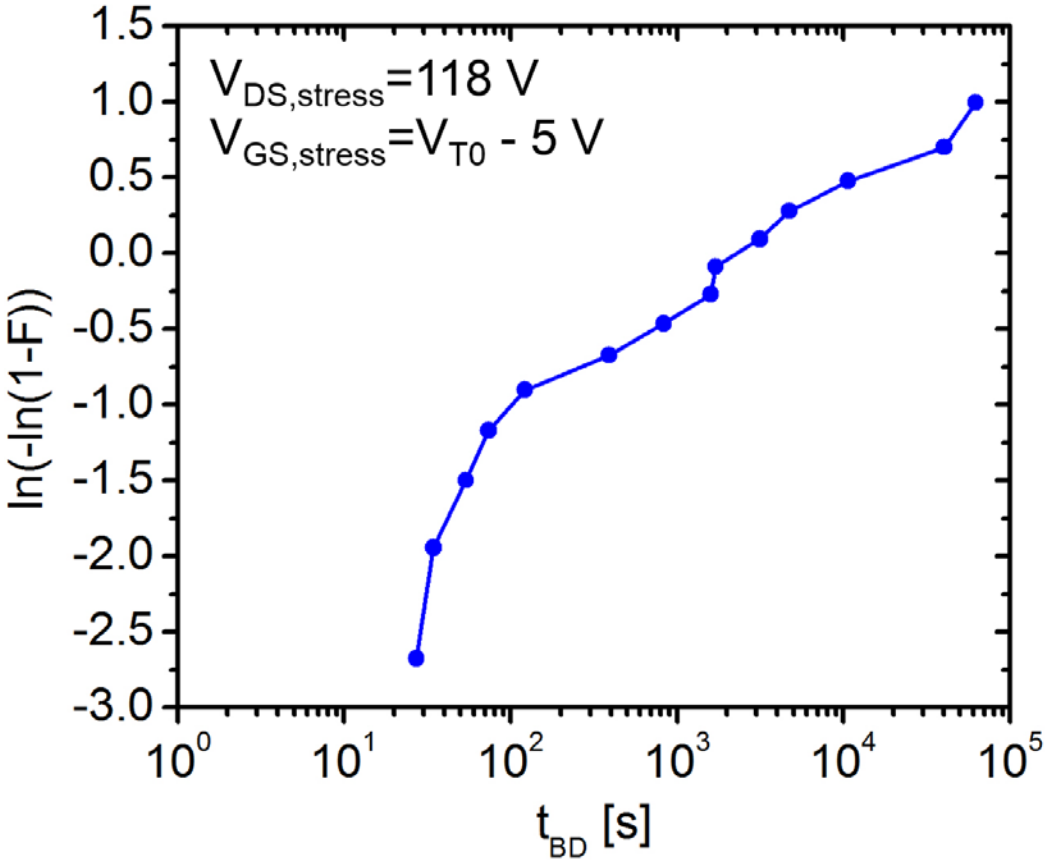
Transfer characteristics in between stress steps

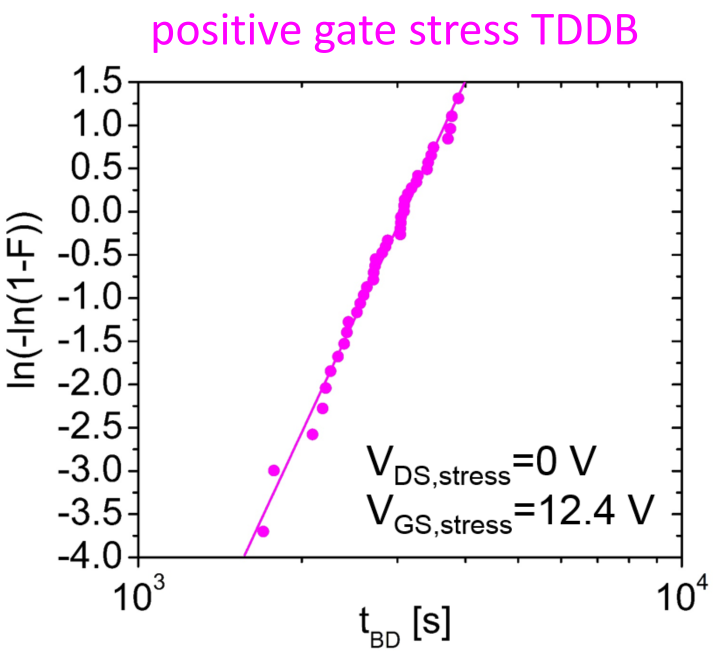


- Very large V_T shifts (first positive, then negative) and hysteresis
- Progressive increase in current collapse for increasing $V_{DS,stress}$

OFF-state TDDB Statistics

Time to final breakdown (I_G=1 mA)





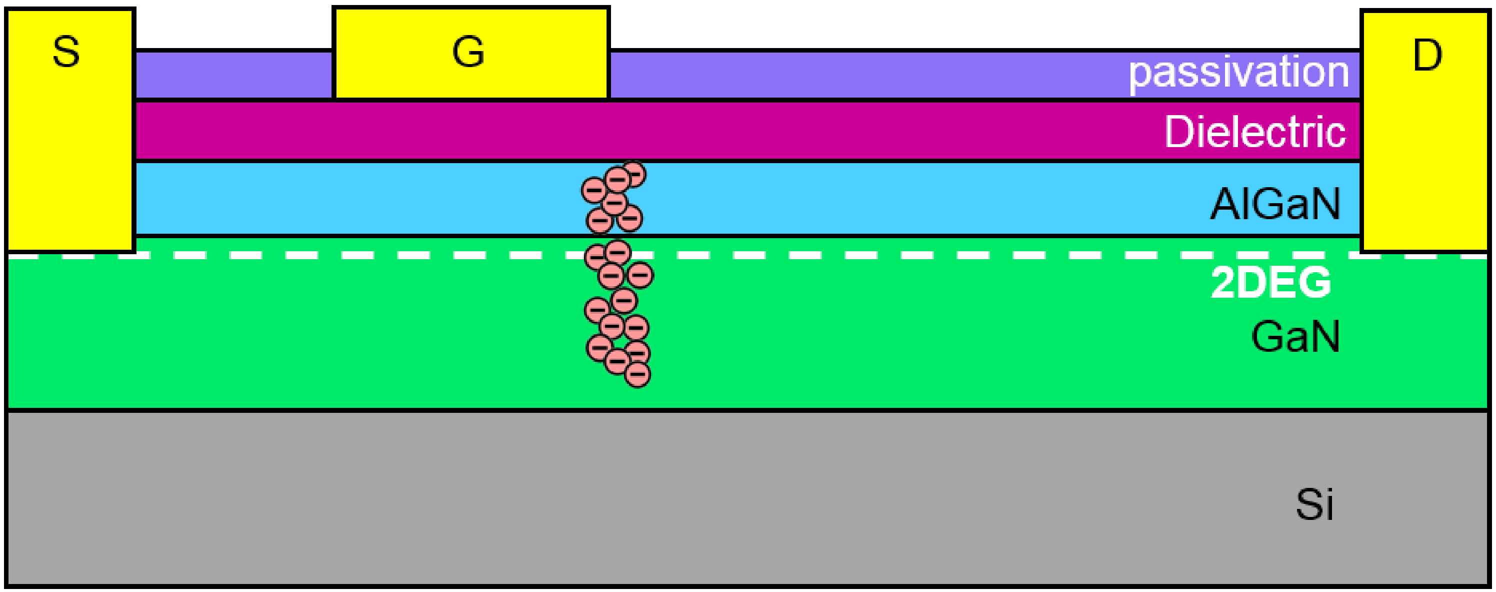
S. Warnock, IRPS 2016

- Statistics do not follow Weibull distribution
- Spread over many orders of magnitude

Trapping at Drain-end of Channel

In OFF-state, large electric field peak at drain-end of channel

→ Severe electron trapping

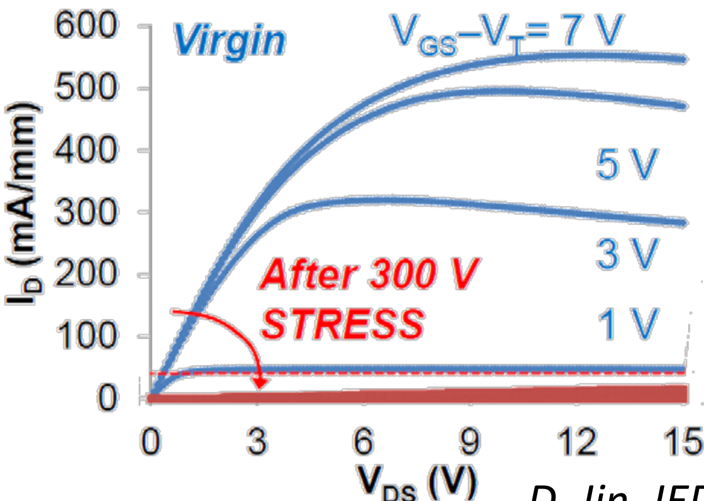


- Trapping affects electric field
- Depends on trap concentration, location, etc.
  → highly random

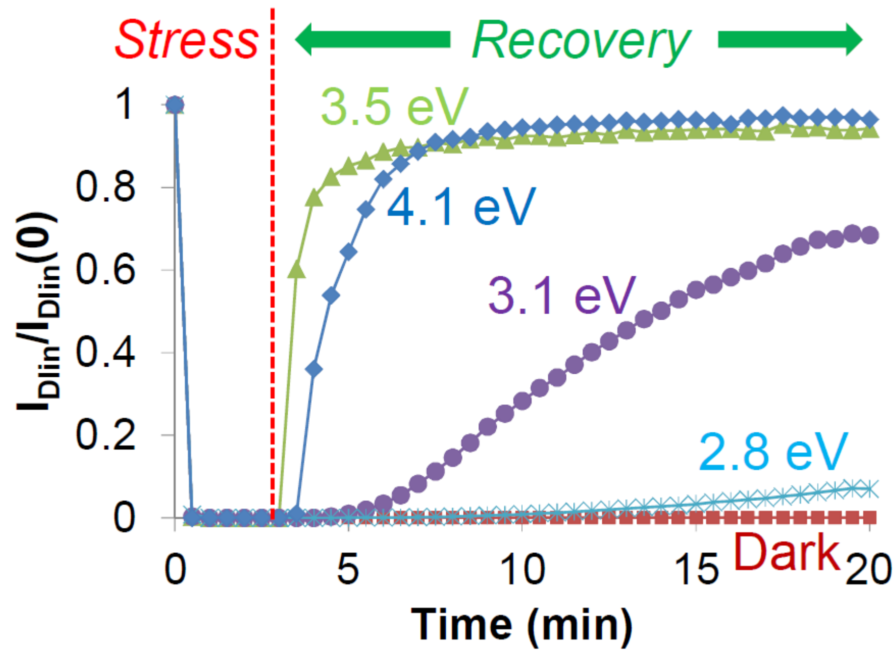
Ultraviolet Light During Recovery & Stress

UV Light to Mitigate Trapping

Need to separate current collapse, V_T shift from permanent degradation



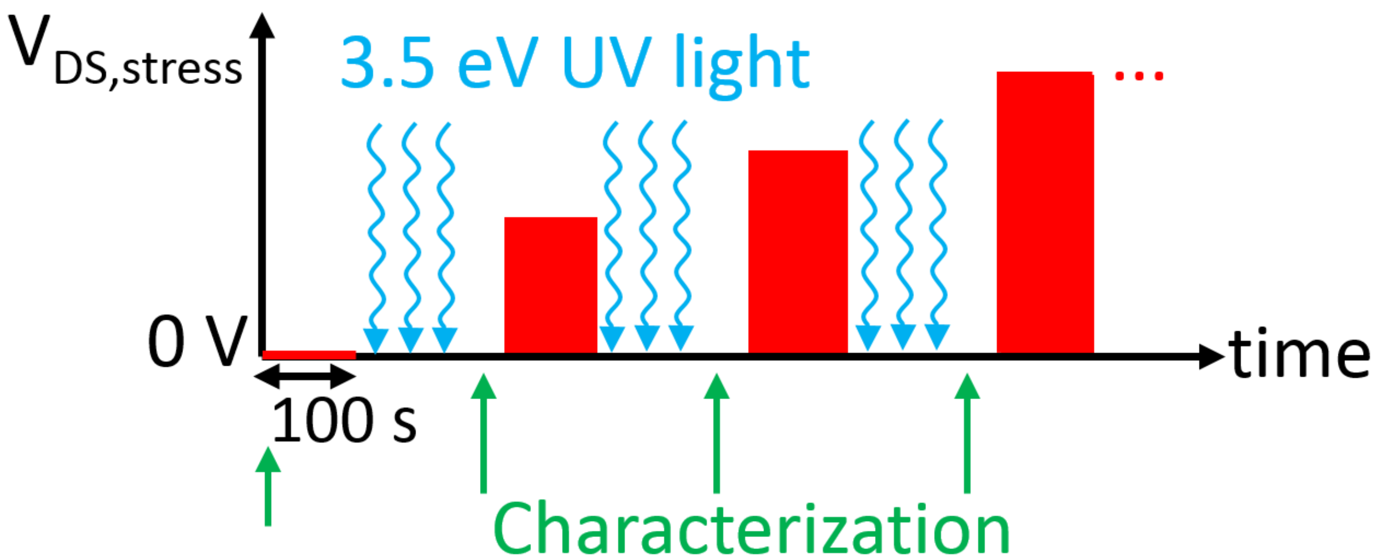
D. Jin, IEDM 2013



- UV light very effective for de-trapping in GaN
- Choose 3.5 eV for TDDB study

OFF-state Step-Stress: Recovery with UV

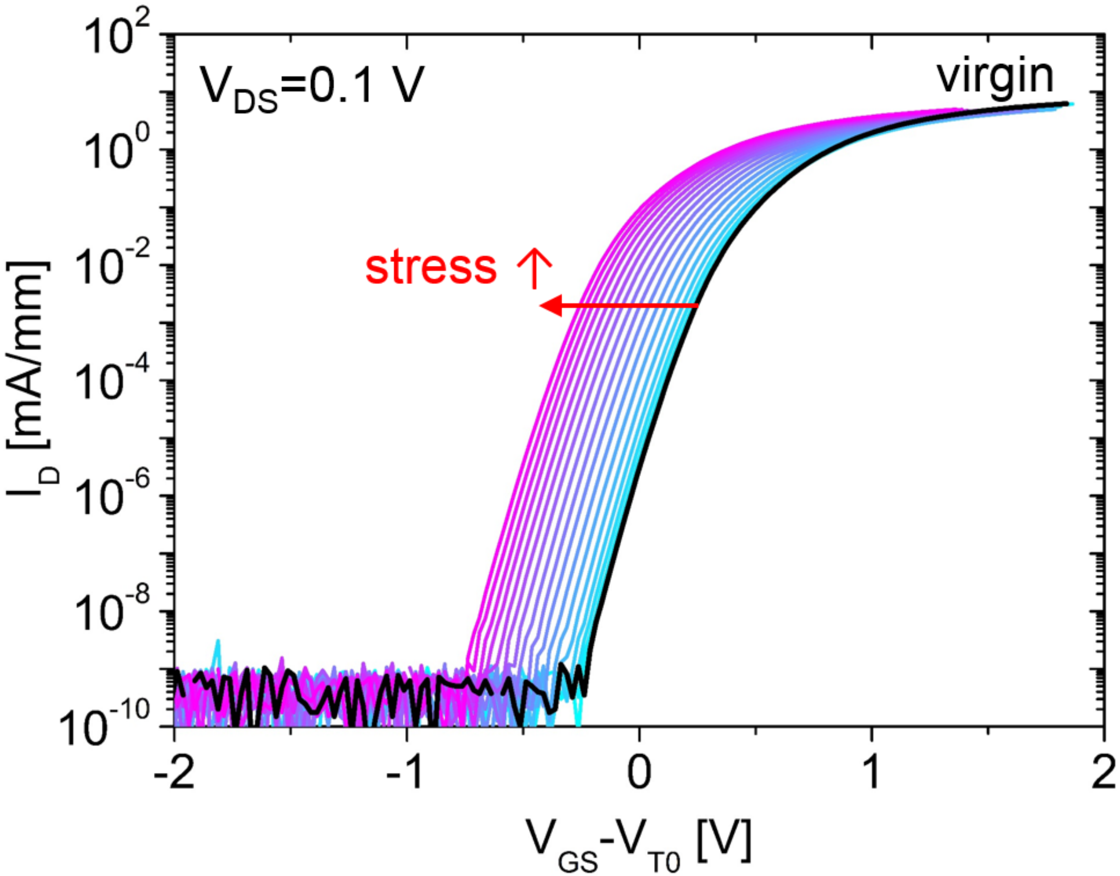
- Step $V_{DS,stress}$: $\Delta V_{DS,stress}$=5 V, each 100 s
- Before characterization, shine 3.5 eV UV light for 5 minutes after each stress step



- No UV during stress → expect unchanged stress leakage current

OFF-state Step-Stress: Recovery with UV

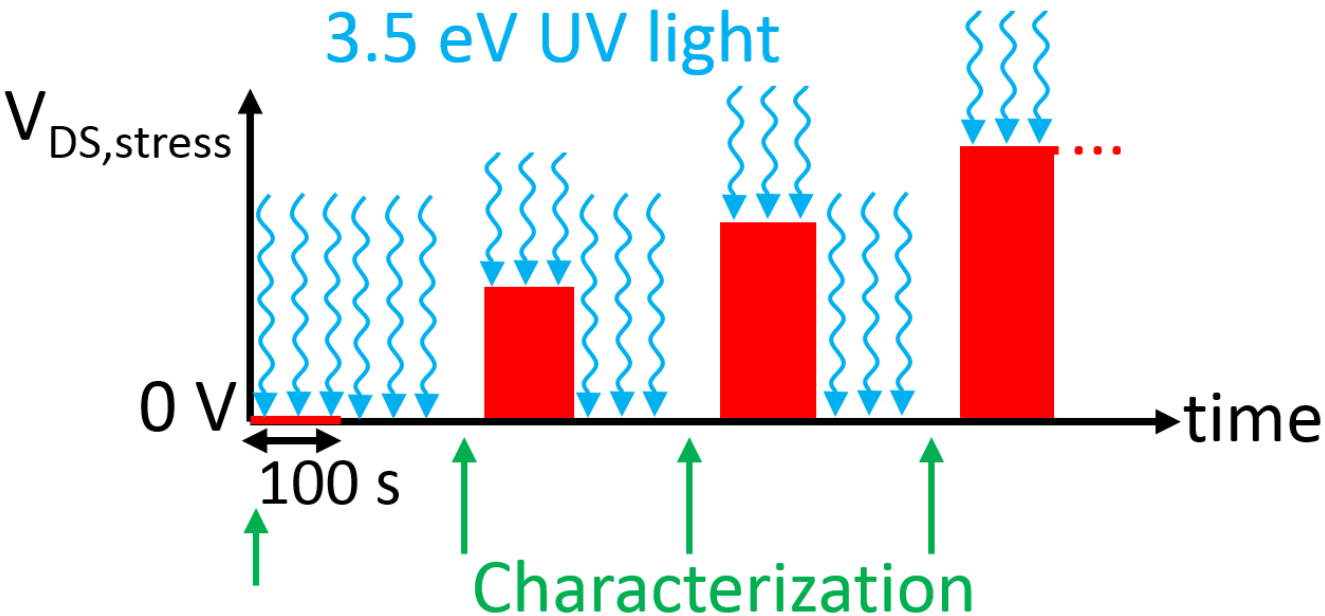
Transfer characteristics in between stress steps



- Current collapse mitigated
- No positive V_T shift, only negative → NBTI

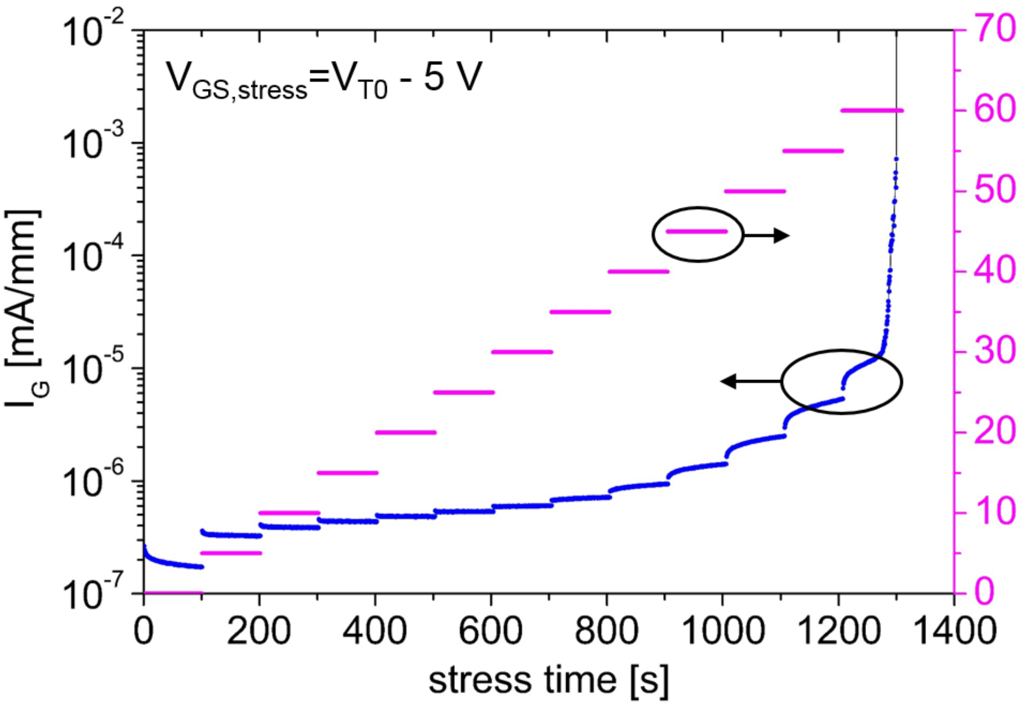
OFF-state Step-Stress: Stress with UV

- Step $V_{DS,stress}$: $\Delta V_{DS,stress}$=5 V, each step 100 s/step
- 3.5 eV UV light during stress, and 5 minutes after (to eliminate residual trapping)

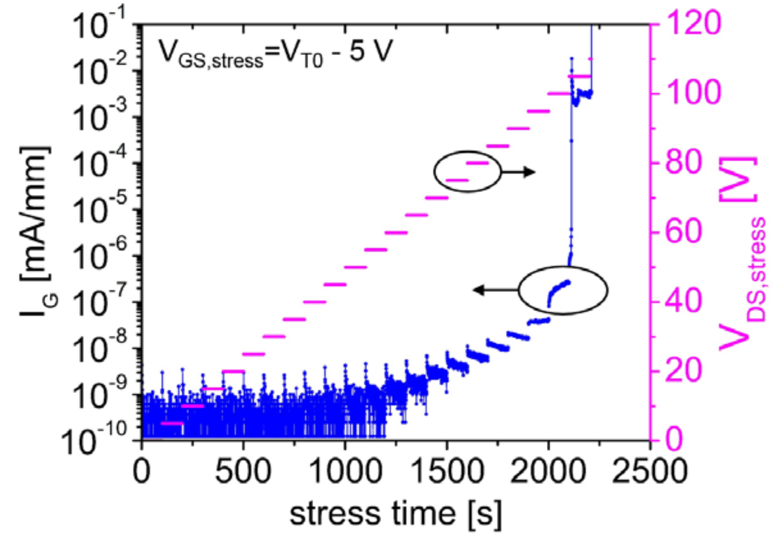


OFF-state Step-Stress: Stress with UV

- Step $V_{DS,stress}$: $\Delta V_{DS,stress}$=5 V, 100 s/step



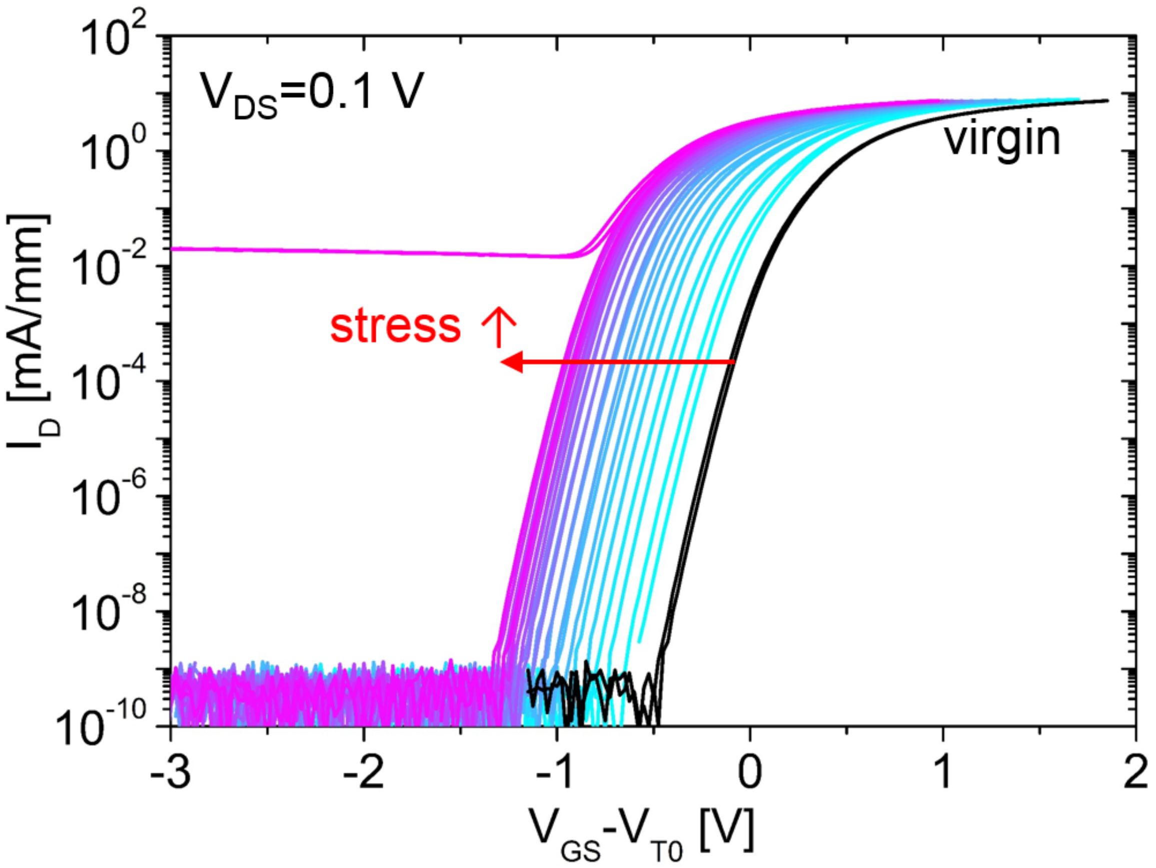
(step-stress in dark)



- No evidence of trapping for moderate $V_{DS,stress}$
- Clear appearance of SILC at higher voltage
- Breakdown at 60 V compared to ~110 V for step-stress in dark

OFF-state Step-Stress: Stress with UV

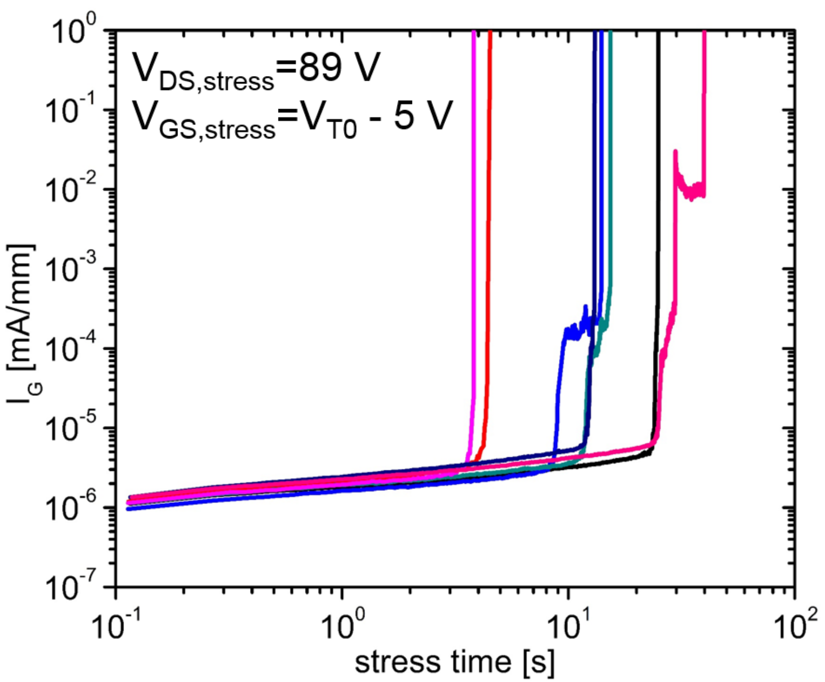
Transfer characteristics in between stress steps

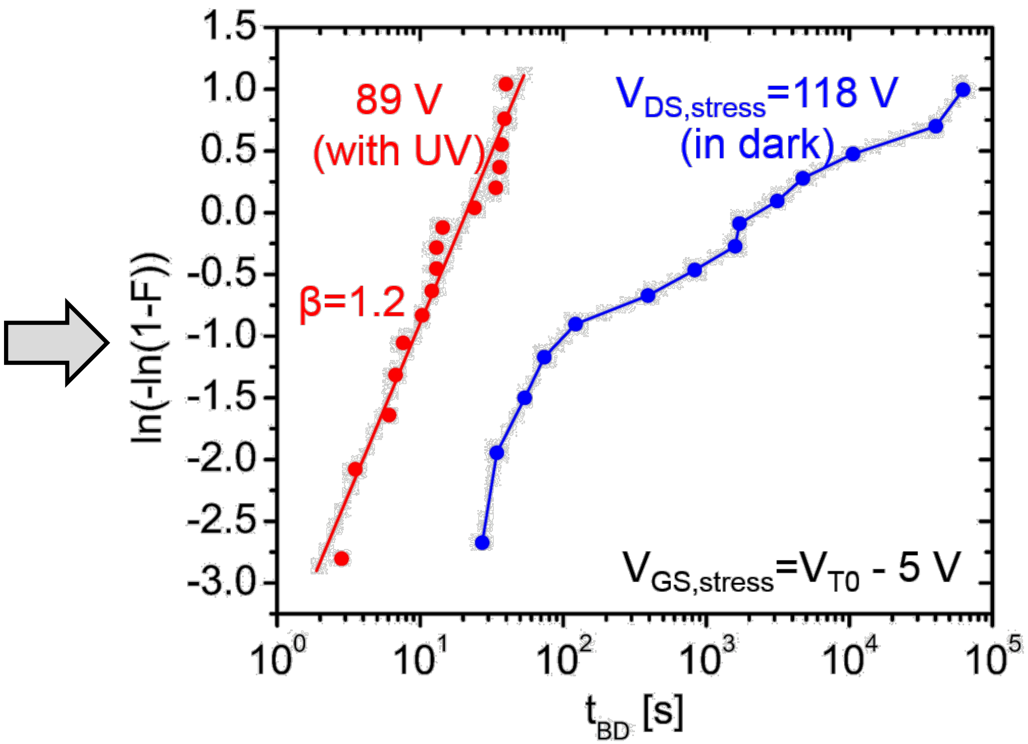


- Current collapse entirely mitigated
- Negative V_T shift → NBTI

OFF-state Constant-Voltage TDDB Statistics

Compare TDDB in the dark and with 3.5 eV UV during stress





- UV statistics now follow Weibull distribution
- Breakdown occurs sooner, even with $V_{DS,stress}$ ~25% less
- UV mitigates trapping → electric field ↑

Conclusions

- Investigated OFF-state TDDB in GaN MIS-HEMTs for the first time
- Without UV light:
  - Current collapse, V_T shift
  - Cannot separate transient and permanent effects
  - Non-Weibull breakdown statistics
- With UV light:
  - Current collapse completed mitigated
  - Progressive negative V_T shift → NBTI
  - UV de-trapping yields higher electric field → accelerated breakdown
  - Breakdown follows Weibull distribution
- Next work: estimate electric field to develop lifetime model

Acknowledgements

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Questions?